

IN THE CLAIMS

1 1. (Original) A signal processor system comprising
2 a power estimation signal,
3 a variable attack and release stage for detecting changes in amplitude of the
4 power estimation signal relative to time,
5 comparing the changes in amplitude relative to time to a first criteria,
6 applying a first algorithm if the change in amplitude does not meet the first
7 criteria,
8 applying a second algorithm if the change in amplitude does meet the first
9 criteria.

1 2. (Original) The signal processor of claim 1 wherein the first algorithm
2 includes a factor representing the amount of compression in the system.

1 3. (Original) The signal processor of claim 1 wherein the first algorithm
2 includes a factor representing the amount of expansion in the system.

1 4. (Original) The signal processor of claim 1 wherein the first algorithm
2 includes a factor representing user preference.

1 5. (Original) The signal processor of claim 1 wherein the detected change in
2 amplitude is positive.

1 6. (Original) The signal processor of claim 1 wherein the detected change in
2 amplitude is negative.

1 7. (Previously presented) The signal processor of claim 5 wherein the first
2 algorithm includes a first factor representing the amount of compression or expansion in
3 the system.

1 8. (Original) The signal processor of claim 7 wherein the first algorithm
2 includes a second factor representing user preference.

- 1 9. (Canceled)
- 1 10. (Original) The signal processor of claim 9 wherein the second algorithm
2 includes a first factor representing the amount of compression or expansion in the system.
- 1 11. (Original) The signal processor of claim 10 wherein the second algorithm
2 includes a second factor representing user preference.
- 3 12. (Original) The signal processor system of claim 1 wherein the power
4 estimation signal comprises a plurality of power estimation signals.
- 1 13. (Original) A variable attack and release processor having an output
2 comprising
3 an input signal,
4 a feedback signal,
5 a comparison stage for providing as a comparison signal a comparison of the
6 input signal and the feedback signal, and
7 a first stage for applying, in accordance with a first characteristic of the
8 comparison signal, a first algorithm, and providing a first stage output signal in
9 accordance therewith.
- 1 14. (Original) The variable attack and release processor of claim 13 further
2 comprising
3 a second stage for modifying the first algorithm in accordance with at least
4 one of a plurality of secondary characteristics, selected from a group comprising
5 at least one of system parameter signals, user preference signals, feedback signal,
6 and a characteristic of the input signal, a second plurality of algorithms.
- 1 15. (Original) The variable attack and release processor of claim 14 wherein the first
2 algorithm includes a plurality of elements in a lookup table.

- 1 16. (Original) The variable attack and release processor of claim 15 wherein the
2 second stage modifies the first algorithm by causing the selection of different entries in
3 the lookup table.
- 1 17. (Original) The variable attack and release processor of claim 14 wherein the first
2 algorithm is generated by combinatorial logic.
- 1 18. (Previously presented) The variable attack and release processor of claim 14
2 wherein the first algorithm comprises a series of computer programming steps.
- 1 19. (Original) The variable attack and release processor of claim 18 wherein the
2 algorithm values are directly calculated.
- 1 20. (Original) The processor of claim 13 wherein the first characteristic is a deviation
2 signal between the current input and the current output.
- 1 21. (Original) The processor of claim 13 wherein the first characteristic is one of a
2 group of logic states comprising attack, release, and a transition between the two.
- 1 22. (Original) The processor of claim 13 wherein the first plurality of algorithms
2 includes filters, linear and non-linear integrators, and time delays.
- 1 23. (Original) The processor of claim 14 wherein the first stage output signal
2 comprises a plurality of processed deviation signals.
- 1 24. (Original) The processor of claim 13 wherein the input signal includes a plurality
2 of incoming signals.
- 1 25. (Original) The processor of claim 13 wherein the feedback signal includes a
2 plurality of feedback signals.
- 1 26. (Original) The processor of claim 13 wherein the comparison stage includes a
2 plurality of comparison sub-stages.

1 27. (Original) The processor of claim 13 wherein the first stage includes a plurality
2 of first sub-stages.

1 28. (Original) The processor of claim 26 wherein the first stage includes a plurality
2 of first sub-stages.

1 29. (Original) The processor of claim 13 wherein the first stage output signal
2 comprises a plurality of coefficients.

1 30. (Original) The processor of claim 14 wherein the first stage output signal
2 comprises a plurality of coefficients resulting from the first stage as modified by the
3 second stage.

1 31. (Original) The processor of claim 13 wherein the comparison stage further
2 outputs at least one variable.

1 32. (Original) The processor of claim 31 wherein the comparison stage further
2 outputs a plurality of control variables.

1 33. (Original) The processor of claim 31 wherein the control variables and
2 coefficients are processed in at least one transform stage in a predetermined manner.

1 34. (Original) The processor of claim 33 wherein the transform stage implements at
2 least one polynomial equation.

1 35. (Original) The processor of claim 33 wherein the transform stage processes the
2 control variables and coefficients in accordance with at least one further lookup table.

1 36. (Original) The processor of claim 33 wherein the transform stage comprises a
2 plurality of sub-transform stages.

1 37. (Original) The processor of claim 36 wherein each of the plurality of sub-
2 transform stages implements a polynomial.

- 1 38. (Original) The processor of claim 37 where each of the polynomials is unique.
- 1 39. (Original) The processor of claim 36 further comprising
- 2 a combiner stage for combining outputs from at least two of the sub-transform stages.
- 1 40. (Original) The processor of claim 13 further including a tracking filter responsive
- 2 to the first stage output signal and having an output.
- 1 41. (Original) The processor of claim 33 further including a tracking filter responsive
- 2 to the output of the transform stage.
- 1 42. (Original) The processor of claim 39 further including a tracking filter responsive
- 2 to the output of the transform stage.
- 1 43. (Original) The processor of claim 33 wherein the output of the tracking filter is a
- 2 combination of the input signal and the feedback signal.
- 1 44. (Original) The processor of claim 33 wherein the output of the tracking filter is
- 2 representative of a power estimate.
- 1 45. (Previously Presented) The processor of claim 44 wherein the power estimate is
- 2 an intermediate power estimate.
- 1 46. (Original) A variable attack and release processor having an output
- 2 comprising an input signal,
- 3 a feedback signal,
- 4 a comparison stage for providing as a comparison signal a comparison of the
- 5 input signal and the feedback signal, and
- 6 a tracking filter responsive to an output of the comparison stage for producing an
- 7 output in accordance therewith.

- 1 47. (Original) The variable attack and release processor of claim 46 wherein the
2 output of the tracking filter is a combination of the input signal and the feedback signal.
- 1 48. (Original) The variable attack and release processor of claim 46 wherein the
2 output of the tracking filter is representative of a power estimate.
- 1 49. (Original) The variable attack and release processor of claim 48 wherein the
2 power estimate signal is an intermediate power estimate.
- 1 50. (Original) The variable attack and release processor of claim 46 wherein the
2 comparison signal is a variable.
- 1 51. (Original) The variable attack and release processor of claim 46 wherein the
2 comparison signal is a logic signal.
- 1 52. (Original) The variable attack and release processor of claim 50 wherein a
2 transform stage receives the comparison signal and provides a transform signal to the
3 tracking filter.
- 1 53. (Original) The variable attack and release processor of claim 51 wherein a first
2 stage receives the comparison signal and provides a first stage output to the tracking
3 filter.
- 1 54. (Original) The variable attack and release processor of claim 46 wherein the
2 comparison signal comprises both a variable and a logic signal.
- 1 55. (Original) The variable attack and release processor of claim 54 wherein a first
2 stage receives the logic signal and provides a first stage output, and the transform stage
3 receives the variable and the first stage output and provides a transform signal to the
4 tracking filter.
- 1 56. (Original) The processor of claim 40 wherein the tracking filter comprises a
2 plurality of tracking filters.

- 1 57. (Original) The processor of claim 41 wherein the tracking filter comprises a
2 plurality of tracking filters.
- 1 58. (Original) The variable attack and release processor of claim 46 wherein the
2 tracking filter comprises a plurality of tracking filters.
- 1 59. (Original) The variable attack and release processor of claim 53 further including
2 a second stage responsive to at least one of a group comprising system parameter signal,
3 user preference signal, feedback signal, and a characteristic of the input signal, for
4 modifying the first stage output.
- 1 60. (Original) The variable attack and release processor of claim 55 further including
2 a second stage responsive to at least one of a group comprising system parameter signal,
3 user preference signal, feedback signal, and a characteristic of the input signal, for
4 modifying the first stage output.
- 1 61. (Original) A signal processor comprising
2 a power estimation signal
3 a variable attack and release stage for detecting changes in amplitude of the
4 power estimation signal relative to time,
5 comparing the changes in amplitude relative to time to a first predetermined
6 threshold,
7 applying a first correction factor if the change in amplitude does not exceed
8 the first predetermined threshold,
9 applying a second correction factor if the change in amplitude exceeds the first
10 predetermined threshold.
- 1 62. (Original) The signal processor system of claim 1 wherein the power
2 estimation signal is a noise signal.

1 63. (Original) The variable attack and release processor of claim 13 wherein the
2 input signal is a noise signal.

1 64. (Original) The variable attack and release processor of claim 46 wherein the
2 input signal is a noise signal.